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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,487	12/22/2000	Steven Tu	42390.P8934	8961

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Michael J. Mallie
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
PATEL, ASHOKKUMAR B	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 09/746,487	Applicant(s) TU ET AL.	
	Examiner Ashok B. Patel	Art Unit 2154	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 31 December 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☒ The Notice of Appeal was filed on *1/11/2006*. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-30*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See continuation sheet..
12. ☒ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). 12/31/2005
13. ☐ Other: _____.

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Continuation sheet:

35 U.S.C. § 103(a) REJECTIONS

Applicant's argument:

Applicant again respectfully submits that while arbitration to identify a first modification request may be resolved on a round-robin basis, the Examiner has not shown any obvious combination to arrive at allowing the first modification request to succeed if the identified ownership state corresponds to the first requesting device, which is precisely what the Examiner has admitted was not disclosed by the cited reference."

Examiner's response:

First of all, this very argument was presented to the Examiner in the previous reply from the Applicant and in response the following was provided which is reiterated here," First of all, Examiner would like to respectfully request the Applicant to refer to Simcoe et al. (US 5, 418, 967), col. 1 through col. 2, line 60 for examples of known arbitration systems including round-robin and priority.

Second, what Examiners had admitted in the previous Office Action is again reiterated here, "Although, the reference Derrick teaches that the first modification request is allowed to succeed if the identified ownership state corresponds to no ownership, and indicates that Bus controller (Arbiter) assigns a priority which determines which semaphore modification request is allowed, the reference fails to explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device, however it is well known in

the art to implement the desired protocol for the priority determining the order of granting the requests for semaphore modifications such as round robin."

As clearly pointed out by Derrick in col. 4, line 35-38, that "Bus controller 402 controls accesses by bus masters 406 to shared resources 408, allowing only one bus master 406 to have control or ownership of any given shared resource 408 at any given time.", and in the same column, line 43-45, Derrick goes on elucidating that " Bus controller 402 may control accesses by bus masters 406 to shared resources 408 using any suitable scheme."

As such, there has to exist "any suitable scheme" in order for Derrick's Bus controller (arbiter) to control access by bus masters (requesting devices) for, as Derrick has stated, "allowing only one bus master 406 to have control or ownership of any given shared resource 408 at any given time." Therefore, Examiner had admitted "the reference fails to explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device" wherein Derrick had failed to specifically point out "any suitable scheme" that will allow its Bus Controller to "allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device."

Applicant's argument:

Accordingly, Applicant respectfully maintains that Derrick does not disclose or suggest the subject matter set forth in Claim 17.

The cited references do not disclose or suggest causing a semaphore checker that receives the semaphore modification requests to identify an ownership state of the

semaphore and to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device.

Instead of a semaphore checker that receives requests, it is Derrick's requesting device that locks out other devices and checks to see if the shared resource is owned by another device. Derrick's device simply locks out accesses by other requesting device to the same semaphore without knowing if it is owned by another master. It is the requesting device of Derrick, rather than a semaphore checker that receives the requests. that checks to see if the shared resource is owned by another device (Fig. 2, steps 204 and 206, co1.,3. lines 57-64)

Examiner's response:

Derrick teaches at col. 5, line 34-51, "Referring again to FIGS. 2 and 5, when a device, such as bus master 406A, needs access to a shared resource (step 102), it initiates a read for ownership (step 202). When **spin buffer** 502 **detects** the read for ownership, **it** looks to see if the information corresponding to the semaphore for the shared resource is already within spin buffer 502. One way of determining whether spin buffer 502 contains the data is to look at the address fields of the memory locations 520. If the address of the semaphore is found within spin buffer 502, and another device does not own the corresponding shared resource, **spin buffer 502 locks out all accesses to the semaphore by other devices** (step 204), and writes to the lock bit/ID field of the memory location 520 (step 210) to indicate that the requesting device now owns the resource corresponding to the semaphore at that address. If the address of the semaphore is found within spin buffer 502 but is owned

by another device, the requesting device must spin and retry later to gain access of the shared resource."

Thus, no, it is not Derrick's requesting device that locks out other devices and checks to see if the shared resource is owned by another device.

Applicant's argument:

"Since the spin buffer of Derrick does not check the ownership state, semaphore access can be granted to a spinning requesting device and denied to the device with ownership (Fig. A col. 3, line 57-67).

On the other hand, a semaphore checker as set forth in Claim I 7, that identifies an ownership state of the semaphore can arbitrate and identify a modification request from a first processor to allow lo succeed . if the ownership state corresponds to the first processor."

Examiner's response:

Derrick teaches at col. 5, line 34-51, "Referring again to FIGS. 2 and 5, when a device, such as bus master 406A, needs access to a shared resource (step 102), it initiates a read for ownership (step 202). When **spin buffer** 502 **detects** the read for ownership, **it** looks to see if the information corresponding to the semaphore for the shared resource is already within spin buffer 502. One way of determining whether spin buffer 502 contains the data is to look at the address fields of the memory locations 520. If the address of the semaphore is found within spin buffer 502, and another device does not own the corresponding shared resource, **spin buffer 502 locks out all accesses to the semaphore by other devices** (step 204), and writes to the lock bit/ID

field of the memory location 520 (step 210) to indicate that the requesting device now owns the resource corresponding to the semaphore at that address. If the address of the semaphore is found within spin buffer 502 but is owned by another device, the requesting device must spin and retry later to gain access of the shared resource."

Thus, the spin buffer of Derrick does not check the ownership state.

Also, as clearly pointed out by Derrick in col. 4, line 35-38, that "Bus controller 402 controls accesses by bus masters 406 to shared resources 408, allowing only one bus master 406 to have control or ownership of any given shared resource 408 at any given time.", and in the same column, line 43-45, Derrick goes on elucidating that " Bus controller 402 may control accesses by bus masters 406 to shared resources 408 using any suitable scheme."

And, in order to further substantiate how the spin buffer arbitrates, Derrick in col. 5, line 52 through col. 6, line 9, "While the embodiment of FIG. 5 shows multiple bus masters 406A-D which access spin buffer 502 through a single bus connection or port 530, the embodiment of FIG. 6 shows a dual-port configuration. According to the second embodiment, bus masters 406A-D access spin buffer 502 through one port 530 to spin buffer 502, while PCI devices 406E and 406F access spin buffer 502 through a second port 540 via PCI bus 550. Spin buffer 502 performs the same basic function as before, but in addition it must discriminate between accesses on each of the two ports 530 and 540. Note that spin buffer 520 has the flexibility to discriminate between individual bus masters (e.g., 406A-406D), or in the alternative, may simply discriminate based on the port on which the device is connected. For example, in the circuit of FIG.

6, spin buffer 502 has a separate ID for each device 406A-406D on port 530, but has a single ID for port 540. Thus, if either of devices 406E or 406F have ownership of a shared resource, the ID that is reflected in the ID field reflects that a device on port 540 has ownership, without distinguishing between the different devices coupled to port 540. Thus, bus master 406A-406D each have a dedicated ID, while bus masters 406E and 406F share an ID. The embodiment as shown in FIG. 6 illustrates that spin buffer 530 may discriminate between individual devices or between ports or between any combination of the two."

Applicant's argument:

"Claim 14 sets forth a multiprocessor system comprising: means for .....first requesting device."

Examiner's answer:

Please refer to the factual evidences provided in the above responses for claim 17.

Applicant's argument:

With regard to claim 24, the spin buffer... claim 24.

Examiner's answer:

Please refer to the factual evidences provided in the above responses for claim 17.